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(54) Alignment method and semiconductor exposure method

(57) Disclosed is an alignment method or an exposure method in an exposure process in which a first stepper having a first reduction magnification and a second stepper having a second reduction magnification, higher than the first reduction magnification, are used in combination. Global alignment of the first stepper is achieved on the basis of a subset of the set of alignment marks defined by the second stepper. The subset comprises alignment marks (60,70) which lie in an annular region between the central and peripheral regions of the wafer (10). The marks occupy a variety of different positions with respect to the exposure field (20) of the first stepper.

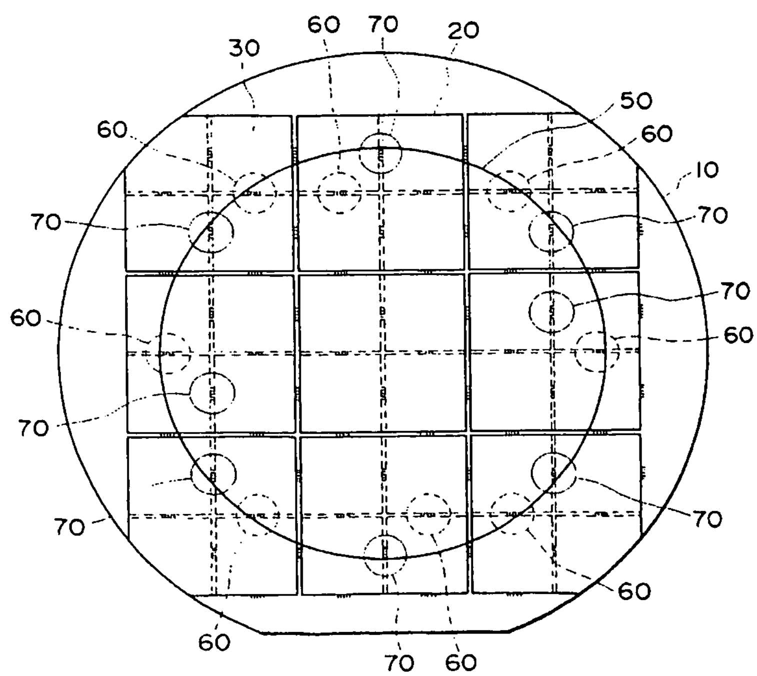

FIG. 1

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Description

FIELD OF THE INVENTION AND RELATED ART

This invention relates to an alignment method in superposition exposure to be used in an exposure process (mix-and-match exposure process) in which exposure apparatuses having different reduction magnifications are used in combination. In another aspect. the invention is concerned with a semiconductor exposure method using a step-and-repeat type or step-and-scan type exposure apparatus. for performing high precision exposure in semiconductor device manufacturing processes. In a further aspect. the invention is concerned with a reticle to be used in such alignment process or semiconductor exposure process.

In some cases of exposure process in the manufacture of semiconductor devices. an exposure apparatus of step-and-repeat type having a reduction magnification of 1:10 to 1:5 (to be called "higher-magnification stepper") and an exposure apparatus of mirror projection type or proximity type of unit magnification, are used in combination (this is called "mix-and-match" process). This is because: A unit-magnification exposure apparatus provides a larger throughput than that of a higher-magnification stepper. In consideration of this, among semiconductor processes of more than ten. the unit-magnification exposure apparatus is used in those processes in which lower resolution or lower alignment precision is required: whereas the higher-magnification stepper is used in those processes in which higher resolution or precision is required. Such mix-and-match procedure is effective to reduce the semiconductor manufacturing cost.

Recently proposed exposure apparatus is a stepper (to be called "lower-magnification stepper) having a reduction magnification of 1:2 to 1:4 and a transfer image size twice larger (four times larger. in terms of area) than that of a higher-magnification stepper.

Now. an exposure process in which a higher-magnification stepper and a lower-magnification stepper are used in combination. will be explained with reference to some of the drawings.

Figure 19 illustrate how to perform global alignment measurement (alignment measurement based on a few selected sample points on a wafer) in a low-magnification stepper. in the mix-and-match procedure. In this case, as seen from Figure 19. those zones on a wafer 410 corresponding to four shots 430 exposed by a higher-magnification stepper are to be exposed by a lower-magnification stepper as one shot 420. Figure 20 illustrates an extracted portion of Figure 19, corresponding to one shot 420 to be exposed by the lower-magnification stepper. Denoted at 440X and 440Y are an X-direction measurement alignment mark and a Y-direction measurement alignment mark, respectively, which have been formed during one shot (exposure) by the higher-magnification stepper.

In a case of global alignment process in which eight peripheral shots of Figure 19 are to be measured, the positions of alignment marks to be measured are fixed with respect to the center of the shot to be exposed by the lower-magnification stepper. as depicted by broken-line circles 460 (marks to be used in X-direction measurement) and solid-line circles 470 (marks to be used in Y-direction measurement). This may cause a necessity of detecting a mark or marks located outside an imaginary circle 450 (having the same center as of the wafer) which depicts a range in which the effect of warp of the wafer or non-uniformness of resist coating of the wafer is small. or it may end in an undesirable result of reduced number of measurements if such outside marks are not measured.

On the other hand. generally a reticle R to be used in a stepper has plural circuit patterns SA - SD (Figure 21) corresponding to plural chips. which are to be exposed by one shot. Also. there are alignment marks as and bs for position detection in respect to X and Y directions, which are placed in peripheral portions (scribe portions) around the exposure zone of one shot. As regards the wafer alignment method. from the viewpoint of balance of productivity and alignment precision, a global alignment method may be used wherein the positions of all the shots of the wafer are determined on the basis of measurements of alignment marks as and bs of a few shots (sample shots) of the wafer and. in accordance with the thus determined positions. the position of each shot of the wafer is adjusted.

SUMMARY OF THE INVENTION

In such mix-and-match procedure as described above in which a higher-magnification stepper and a lower-magnification stepper are used in combination. since the lower-magnification stepper has a larger picture field size per one shot, the number of exposures (exposure operations) per one wafer is smaller than that by the higher-magnification stepper. This raises a problem that. when alignment measurement is performed by selecting a few sample points on a wafer. the number of sample points becomes smaller which may lead to decreased alignment precision. Also. a large span can not be defined between alignment marks. and the alignment precision may be degraded.

Further. since the positions of alignment marks to be measured are fixed with respect to the center of the shot to be exposed by the lower-magnification stepper. there is a possibility that some alignment marks are located at a peripheral portion of the wafer, this being undesirable in the point of higher sensitivity to warp of the wafer or to a change in film thickness of a resist. Thus. the alignment precision may be degraded.

In this respect. it is an object of the present invention to provide an alignment method by which accurate alignment process is assured without degradation of alignment precision even if the sample points are not many

or if the span of alignment marks is not large.

In addition. the exposure field size of each shot of steppers has become larger. As a result of this, the number of step-and-repeat motions of a wafer (generally corresponding to the number of shots) has become very small. This is a factor for restricting the selection of sample shots and for causing deterioration of the alignment precision.

Figure 22 shows an exposure layout in such case. The illustrated is an example wherein a reticle R shown in Figure 21 is used in combination with a wafer 41 of 8-inch diameter and with an exposure size of 50 mm square, and the layout and positions of alignment marks as and bs of each shot are depicted. In this example. as illustrated, only sixteen (16) shots are defined on the wafer 41. Further, in regard to those shots which are at an outside peripheral portion of the wafer, there is a high possibility of non-uniformness in film thickness of a resist or distortion of the wafer. In consideration of them, as the sample shots for global alignment, only four shots 1s - 4s about the center may be selected. The span between the alignment marks is very short as of about 50 mm, and the number of the sample shots is only four. As a result. the precision of measured values in relation to rotation or magnification of the shot layout of the wafer would be degraded.

Shots 2s, 3s. 5s and 6s may be selected as the sample shots in a attempt to obtain a long span of alignment marks. In that occasion, however, the mark positions are not symmetric with respect to the wafer center, and this undesirably creates an error factor. Further. in different shots the mark position may be made different. In that occasion. however. a measurement error may occur due to distortion of an exposure optical system, for example. Such error directly leads to a factor of degradation of the alignment precision, and it is not desirable too.

Another object of the present invention is provide a semiconductor exposure method and/or a reticle by which accurate alignment is assured.

In accordance with an aspect of the present invention. there is provided an alignment method in an exposure process in which a first stepper having a first reduction magnification and a second stepper having a second reduction magnification. higher than the first reduction magnification. are used in combination, characterized in that: for a global alignment through the first stepper on the basis of alignment marks having been defined through the second stepper in relation to shots thereof. in every shot of the first stepper the position of such alignment mark or marks to be measured is made variable with respect to the shot center.

In one preferred form of this aspect of the present invention. in the global alignment through the first stepper, the same alignment mark to be used in global alignment through the second stepper is measured.

In accordance with another aspect of the present invention. there is provided an alignment method in an exposure process in which a first stepper having a first reduction magnification and a second stepper having a second reduction magnification, higher than the first reduction magnification. are used in combination. characterized in that: for a global alignment through the second stepper on the basis of alignment marks having been defined through the first stepper, in every shot of the second stepper the position of such alignment mark or marks to be measured is made variable with respect to the shot center.

In one preferred form of this aspect of the present invention, alignment marks defined through the first stepper are placed symmetrically with respect to the shot center of the first stepper. and wherein the global alignment through the second stepper uses the thus symmetrically placed alignment marks the number of which is even for different shots.

In another preferred form of this aspect of the present invention, alignment marks of a shot of the first stepper are placed symmetrically in a direction of measurement and with respect to the shot center, and wherein the number of alignment marks to be measured in relation to the symmetrical pair is even.

In accordance with a further aspect of the present invention. there is provided an alignment method in an exposure process in which alignment marks are formed on a substrate and in which a first stepper having a first reduction magnification and a second stepper having a second reduction magnification, higher than the first reduction magnification, are used in combination, characterized in that: offsets are set on the basis of image heights of alignment marks of a shot, and wherein the set offset are reflected in accordance with the number of alignment marks at each image height as measured.

Briefly. in accordance with the present invention, a first stepper having a first reduction magnification and a second stepper having a second reduction magnification, higher than the first reduction magnification. may be used in combination, and, for a global alignment through the first stepper on the basis of alignment marks having been defined through the second stepper in relation to shots thereof. in every shot of the first stepper the position of such alignment mark or marks to be measured may be made variable with respect to the shot center. This allows that an alignment mark or marks to be measured are located at the position where the effect of wafer warp or a change in resist film thickness is small.

The global alignment through the first stepper. the same alignment mark to be used in global alignment through the second stepper may be measured. This provides a larger latitude for setting the alignment mark position, and the alignment mark span can be made large. Thus, it is effective to prevent degradation of alignment precision. Also, the number of shots to be measured in the global alignment can be made larger than the number of shots to be exposed by the first stepper having a lower reduction magnification. and thus reduction

in number of sample shots can be prevented.

The alignment marks defined through the first stepper may be placed symmetrically with respect to the shot center of the first stepper, or they may be made symmetrically with respect to the shot center only in relation to the measurement direction. Also, the global alignment through the second stepper may use the thus symmetrically placed alignment marks the number of which may be even for different shots. This is effective to avoid the effect of aberration of distortion.

Offsets may be set on the basis of image heights of alignment marks of a shot, and the set offset may be reflected in accordance with the number of alignment marks at each image height as measured. In that occasion, deviation of each alignment mark from the image height may be calculated, and the result may be taken as an offset. This is effective 'to reduce the effect of aberration of distortion.

In accordance with a further aspect of the present invention, there is provided a reticle to be used in a semiconductor exposure apparatus and having a pattern of plural chips to be exposed in relation to a single shot, characterized in that: the reticle is provided with an alignment mark in relation to each of the chips.

In accordance with a still further aspect of the present invention, there is provided an exposure method for performing sequential exposure of different shot regions of a substrate, comprising the steps of: performing an exposure process to the substrate by use of a reticle having plural chip patterns, to be exposed in a single shot, and alignment marks provided in relation to the chip patterns, respectively; and performing an alignment process to the substrate by using an alignment mark in each chip as transferred to the substrate through said exposure process.

In one preferred form of this aspect of the present invention, in each shot on the substrate, a position measurement error produced in dependence upon the position of an alignment mark with respect to the shot center is measured and wherein a measured value of each alignment mark position with respect to the shot center is corrected on the basis of the error measurement.

In accordance with a yet further aspect of the present invention, there is provided an exposure method for performing sequential exposure of different shot regions of a substrate, comprising the steps of: performing an exposure process to the substrate by use of a reticle having plural chip patterns, to be exposed in a single shot, and alignment marks provided in relation to the chip patterns, respectively; and measuring at least one of a chip magnification error and a chip rotation, by using an alignment mark in each chip as transferred to the substrate through said exposure process.

In one preferred form of this aspect of the present invention, each chip of the reticle is provided with two opposed alignment marks for X-direction detection and two opposed alignment marks for Y-direction detection, which are disposed around that chip.

Briefly, in these aspects of the present invention, even in a case of large field size exposure in which one shot zone is large because each chip has an alignment mark pattern or patterns, there is a large latitude of alignment mark selection.-Therefore, as compared with conventional processes wherein an alignment mark or marks are provided only in relation to the shot, it is possible to provide a larger distance between alignment marks to be measured 'for the global alignment. Also, selection of such alignment marks having higher symmetry with respect to the wafer center, is assured. Thus, enhanced alignment precision is provided. In that occasion, a position measurement error may occur, depending on the position of the alignment mark in the shot zone with respect to the shot center. Thus, such error may preferably be memorized beforehand and, on the basis of this, the measured value of the alignment mark position with respect to the shot center may be corrected. This assures further enhancement of the alignment precision.

Magnification error of a shot or a chip rotation in that shot may be measured by using the position of alignment marks in plural chips of that shot. By correcting such error or rotation, more correct exposure is assured.

These and other objects, features and advantages of the present invention will become more apparent upon a consideration of the following description of the preferred embodiments of the present invention taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic view for explaining global alignment measurement in a lower-magnification stepper, in an alignment method according to an embodiment of the present invention.

Figure 2 illustrates an extracted portion of Figure 1, corresponding to a single shot of the lower-magnification stepper.

Figure 3 is a schematic view for explaining global alignment measurement in a higher-magnification stepper, in an alignment method according to an embodiment of the present invention.

Figure 4 illustrates an extracted portion of Figure 3, corresponding to a single shot of a lower-magnification stepper.

Figure 5 is a schematic view for explaining the number of measurements (measurement times) at each measurement position in Figure 4.

Figure 6 is a schematic view for explaining an example, in relation to the embodiment of Figure 3, where aberration of distortion is not taken into account.

Figure 7 illustrates an extracted portion of Figure 6, corresponding to a single shot of a lower-magnification stepper.

Figure 8 is a schematic view for explaining the number of measurements (measurement times) at each

measurement position in Figure 7.

Figure 9 is a schematic view for explaining global alignment measurement through a higher-magnification stepper, in an alignment method according to an embodiment of the present invention, particularly in an occasion where the size of one shot of a lower-magnification stepper is not n-times larger (n is an integer) than that of the higher-magnification stepper.

Figure 10 illustrates an extracted portion of Figure 9, corresponding to a single shot of the higher-magnification stepper.

Figure 11 illustrates an extracted portion of Figure 9, corresponding to a single shot of the lower-magnification stepper.

Figure 12 is a plan view of a reticle according to an embodiment of the present invention.

Figure 13 is a schematic view for explaining layout in an occasion where the reticle of Figure 12 is used with a stepper for exposure of a wafer.

Figure 14 is a plan view of a reticle according to another embodiment of the present invention.

Figure 15 is a schematic view for explaining layout in an occasion where the reticle of Figure 14 is used with a stepper for exposure of a wafer.

Figure 16 is a plan view of a reticle according to a further embodiment of the present invention.

Figure 17 is a schematic view for explaining layout in an occasion where the reticle of Figure 16 is used with a stepper for exposure of a wafer.

Figure 18 is a schematic view of a semiconductor device manufacturing projection exposure apparatus to which the present invention is applicable.

Figure 19 is a schematic view for explaining global alignment measurement through a lower-magnification stepper, in conventional mix-and-match procedure.

Figure 20 illustrates an extracted portion of Figure 19, corresponding to a single shot of the lower-magnification stepper.

Figure 21 is a plan view of a reticle of known type.

Figure 22 is a schematic view for explaining layout in an occasion where the reticle of Figure 21 is used with a stepper for exposure of a wafer.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

First, the structure of a step-and-repeat type (or step-and-scan type) projection exposure apparatus, called a stepper, to which the present invention is applicable, will be explained with reference to Figure 18. Denoted in the drawing at 100 is an illumination optical system which produces exposure light with which a pattern (including plural 'chip patterns) formed on a reticle 101 is to be projected and lithographically transferred to a photosensitive resist layer, applied to a wafer 1. Denoted at 102 is a reticle stage for holding the reticle 101. In response to projection of exposure light from the illumination optical system 100 to the reticle 101 as held by the reticle stage 102, the pattern of the reticle 101 is projected, through a reduction projection lens 103 and in a reduced scale, upon a wafer 1 which is held by a wafer chuck 106. In this Specification, the term "higher-magnification stepper" refers to a stepper with a projection lens 103 having a projection magnification of about 1:9 to 1:10, while the term "lower-magnification stepper" refers to a stepper with a projection lens 103 having a unit projection magnification 1:1 or a projection magnification of about 1:2 to 1:4.

Denoted at 104 is an autofocusing system of known structure. It serves to project a light beam onto the surface of the wafer 1, and to detect the position of the wafer surface in the direction of optical axis (Z axis) and with respect to the focusing plane of the projection lens 103 by photoelectrically detecting reflected light from the wafer surface. On the basis of detection by the autofocusing system, the wafer chuck 106 is moved by a driving mechanism (not shown) in the optical axis direction of the projection 'lens 103 such that the surface of the wafer 1 is placed at the focusing plane of the projection lens 103. Denoted at 107 is a wafer stage for moving the wafer 1, held by the wafer chuck 106, along a plane (X-Y plane) perpendicular to the optical axis direction of the projection lens 103. Particularly, it serves to cause step-and-repeat motion of the wafer 1 in the process of sequential exposures of zones of the wafer 1.

Denoted at 108 is a mirror which is movable together with the wafer stage 107 along the X-Y plane, and denoted at 109 is a laser interferometer type distance measuring system of known structure, for measuring the position of the wafer stage 107 upon the X-Y plane, in combination with the mirror 108. Denoted at 110 is a console unit which serves to control the projection exposure apparatus as a whole. Denoted at 111 is an alignment detecting system of known structure, for detecting an alignment mark or marks, formed on the wafer 1, through the projection lens 103 and for measuring the position of the wafer 1 with respect to the X-Y plane. The console unit 110 functions on one hand to control the projection exposure apparatus as a whole and, on the other hand, it serves to determine and select sample shots (alignment marks to be measured), to be described later. In the following description, unless mentioned 'otherwise specifically, determination is performed under the control by a central processing unit (CPU) of the console unit 1.

Figure 1 is a schematic view for explaining global alignment measurement process with a lower-magnification stepper, in an embodiment of alignment method of the present invention. As seen in Figure 1, those zones corresponding to four shots 30 as exposed by a higher-magnification stepper having a reduction magnification of about 1:4 to 1:10 is to be exposed by a single shot 20 of a lower-magnification stepper having a reduction magnification 1:1 to 1:4. Figure 2 corresponds to an extracted portion of Figure 1, corresponding to one shot 20 of the lower-magnification stepper.

In this embodiment, for the global alignment procedure through the lower-magnification stepper, out of the alignment marks $40X_1$ -$40X_4$ and $40Y_1$ - $40Y_4$ having been formed in the exposure processes by the higher-magnification stepper in relation to the shots 30 on the wafer 10, one alignment mark is selected in relation to the X direction and one alignment mark is selected in relation to the Y direction, the selection being made in relation to every shot 20 to be exposed by the lower-magnification stepper, such that the positions of the marks to be used as the subject of measurement can be set variable with respect to the center of the shot 20.

More specifically, the positions of the marks to be used as the subject of measurement are indicated in Figure 1 by broken-line circles 60 (marks to be used in X-direction measurement) and solid-line circles 70 (marks to be used in Y-direction measurement). As seen in the drawing, those marks which are inside an imaginary circle 50, depicting a range in which there is a small effect of warp of the wafer 10 or of non-uniformness of resist coating, and which are located at an outside portion within that range, are selected. After the selection, the wafer stage 107 is moved along the X-Y plane in accordance with signals from the console unit 110, so that the selected alignment marks are placed sequentially at the-position whereat the mark is detected by the alignment detecting system 111. Thus, measurements of global alignment procedure start.

This ensures minimization of the effect of non-uniformness of the resist coating or of wafer warp particularly at the peripheral portion of the wafer. Additionally, it is possible to define a maximum span of those alignment marks selected as the subject of measurement. As a result, good alignment precision is obtainable.

Figure 3 is a schematic view for explaining global alignment measurement process with a higher'magnification stepper, in an embodiment of alignment method of the present invention. Figure 4 corresponds to an extracted portion of Figure 3, corresponding to one shot 20 of a lower-magnification stepper. In this embodiment, as compared with the preceding embodiment, the shot layout for the lower-magnification stepper is such that lateral rows have a mutual shift by a half pitch. In this example, the global alignment procedure through the higher-magnification stepper is to be performed by using alignment marks having been exposed by the lower-magnification stepper in relation to the shots thereof.

In this embodiment, alignment marks to be exposed by the lower-magnification stepper are placed symmetrically with respect to the optical axis center 180 (shot center) of the reduction projection lens 103 (Figure 18), as that shot in which those alignment marks are to be exposed is disposed at the exposure position. Additionally, as regards the alignment marks to be used in the global alignment procedure through the higher-magnification stepper, the same number of measurements is set to these marks with respect to the optical axis center 180 of the reduction projection lens 103. In Figure 3, denoted at 110 is a wafer, and denoted at 120 is a zone corresponding to a single shot by the lower-magnification stepper. Denoted at 130 is a zone corresponding to a single shot of the higher-magnification stepper. The positions of alignment marks to be used in the global alignment procedure through the higher-magnification stepper are depicted by broken-line circles 160 (X-measurement) and solid-line circles (Y measurement).

According to "Lens Design Method" by Yoshiya Matsui, published by Kyoritsu Shuppan, Japan, 1972, the aberration of distortion is proportional to cubic of field angle (in aberration explosion up to cubic). Namely, where the marks $140X_1$, $140X_2$, $140Y_1$ and $140Y_2$ shown in Figure 4 are placed symmetrically with respect to the optical axis center 180 of the reduction lens 103 and where the set number of measurements (measurement times T) at each alignment mark position within every sample shot 120 is even, the effect of aberration of distortion is canceled. In this example, the number T of measurements at each alignment mark position within every sample shot 120 is "four".

Figure 6 corresponds to a case where aberration of distortion is not taken into account. Figure 7 illustrates an extracted portion of Figure 6, corresponding to a single shot by the lower-magnification stepper. Figure 8 illustrates the number of measurements at respective measurement positions in Figure 7.

Without taking into account the aberration of distortion, the number of measurements is not even such that, as illustrated in Figure 8, for a mark $240X_1$ and a mark $240X_2$ the measuring operation is performed three times ($T=T_3$) and once ($T=T_1$), respectively. Thus, due to the effect of aberration of distortion, the alignment precision may decrease. For marks $240Y_2$ and $240Y_3$, the measuring operation is performed for times ($T=T_4$). For marks $240X_3$ and $240X_4$, the measuring operation is performed twice ($T=T_2$).

In the example of Figure 5, the X-direction measurement and the Y-direction measurement are performed by using separate marks (to be called "X-Y split mark"). However, such a mark by which both of the X-direction and Y-direction measurements are attainable, may be used. When an X-Y split mark is used and if the number of measurements set to the ma[illegible]s even, it is not a requisition that the split mark is placed exactly symmetrically with respect to the center 180 (Figure 4) of the reduction projection lens 103. Approximate symmetry may be sufficient.

As a pair of marks $140X_3$ and $140X_4$ such as shown in Figure 4, for example, those marks which are placed off the axis may be used provided that they are disposed symmetrically in respect to the direction in relation to which the measurement is to be done. Also, the aberration of distortion of the reduction projection lens may be measured beforehand, and alignment marks may be provided at those positions where the aberration of distortion can be canceled.

In a case where positions of alignment marks on a

wafer are deviated due to the aberration of distortion of the reduction projection lens. the amount of deviation of each alignment mark from the image height where the mark should be may be measured so that offset information may be prepared with respect to these alignment marks. Such offset information may determined on the basis of measurement of aberration of distortion of the reduction projection lens. Alternatively, a reference wafer may be used: That is. a global alignment procedure may be performed. for example. in a combination of alignment marks $40X_i$ and $40Y_j$ (i = j. i = 1 to 4) and, in relation to each i or j, an alignment offset may be detected. The alignment offset may be one reflecting the times the mark is used. As regards use of the image height based alignment offset described above. it may be used not only in a case where global alignment procedure is performed through a higher-magnification stepper by using alignment marks exposed through a lower-magnification stepper but also in a case where global alignment procedure is performed through a lower-magnification stepper by using 'alignment marks exposed through a higher-magnification stepper. Also, it may be used in a case where, while alignment marks are disposed at different image heights and exposed through a lower-magnification stepper, global alignment procedure is performed through the lower-magnification stepper by using the alignment marks at different image heights.

Figure 9 is a schematic view for explaining mix-and-match procedure according to a further embodiment of the present invention, wherein global alignment measurement is to be performed through a higher-magnification stepper in an occasion where the size of a single shot of a lower-magnification stepper is not n-times (n is an integer) larger than that of the higher-magnification stepper. Figure 10 shows an extracted portion of Figure 9. corresponding to a single shot of the higher-magnification stepper. Figure 11 shows an extracted portion of Figure 9, corresponding to a single shot of the lower-magnification stepper.

In this embodiment, as shown in Figure 9. a substrate layer is formed by using the higher-magnification stepper and then the alignment operation is effected through the lower-magnification stepper. In the higher-magnification stepper. as shown in Figure 10. there are plural chips per one shot (six chips in the Figure 10 example) and. in regard to each of X-direction and Y-direction measurements. there is one alignment mark $340X_1$ or $340Y_1$. Each cross denotes the shot center of the higher-magnification stepper. In a case as shown in Figure 9 where the size of one shot of the lower-magnification stepper is not n-times larger (n is an integer) than that of the higher-magnification stepper. the layout for exposure process through the lower-magnification stepper will be such as shown in Figure 9 wherein each shot partially overlap some shots of the higher-magnification stepper. In the global alignment procedure to be performed prior to it, alignment marks are selected in regard to the shot layout as determined by the higher-magnification stepper. For example. when alignment marks of those shots as denoted by double circles, a sufficiently wide alignment mark span can be defined and. additionally. the number of marks is not insufficient. As regards the alignment mark setting in this embodiment. the setting is not limited to the one shown in Figure 9. Only necessary is that at least one mark is set in relation to one shot of the lower-magnification stepper.

Figure 12 is a plan view of a reticle according to an embodiment of the present invention, which is to be used in a lower-magnification stepper. As shown in the drawing, this reticle is provided with chip patterns S_A - S_D and, in relation to each chip pattern, there are alignment marks a and b for X-direction measurement and Y-direction measurement, respectively. Figure 13 is a plan view for explaining the layout and the disposition of the alignment marks a and b in a case where the above-described reticle is to be used with an exposure size of 50 mm square and with a wafer of 8-inch diameter.

In conventional global alignment process. only the alignment marks at four central shots can be used. In this embodiment, as shown in Figure 13. it is possible to perform the measurement while using the alignment marks a and b of the chips 1 - 8 as sample shots (sample chips). Namely. the alignment mark selection in the shot can be done in the unit of chip. As a result, the number of sample shots (sample chips) can be four (4) to eight (8). Additionally, a longer alignment mark span can be defined. As regards the sample chip, while the chip pattern may be eclipsed in the outside peripheral portion of the wafer. if measurement is done to the alignment marks of the chips 9 - 12 in which the alignment marks a and b are exposed. it is possible to further extend the alignment mark span and, thus, to ensure further improvements in precision.

In the preceding embodiment, as shown in Figure 13. the alignment marks a and b at chips 1 - 8 are placed at different positions with respect to the 'shot center. For example, in shot B-I at column B and row I, the alignment marks a and b of the chip 1 are at lower left side of the center. In shot A-II. the alignment marks a and b are at upper right side of the center. Thus, due to distortion of the exposure optical system (projection lens 103). for example. the alignment mark position a or b with respect to the shot center may be different in several shots. This is a factor of alignment error.

In this embodiment. the following correction is made to improve the alignment precision. That is. the amount of distortion of the exposure optical system is memorized in a table beforehand. Then, in regard to a mark position x as measured, the amount α (%) of the distortion corresponding to that position is read out of the table. and a correction amount αx is determined. In this manner. regardless of the alignment mark position within the shot, it is possible to calculate the shot center accurately and, therefore. to attain enhanced alignment

precision.

Figure 14 is a plan view of a reticle according to another embodiment of the present invention. When a step-and-repeat exposure process is to be done by using a stepper. generally there occurs an error in magnification (to be called "chip magnification error") due to the exposure optical system or rotation (to be called "chip rotation") due to an error in movement of a stage such as the wafer stage 107 of Figure 18. These two error factors become particularly notable in a large-field exposure stepper. In this embodiment. in consideration thereof, as shown in Figure 14 there are provided X-direction position detecting alignment marks a and a' and Y-direction position detecting alignment marks b and b', around chips S_A - S_D.

Figure 15 is a plan view for explaining the layout in a case where an 8-inch wafer is exposed by using the above reticle. In regard to shot B-II, the positions of alignment marks a of the chips S_A and S_B (or alignment marks a' of chips S_C and S_D) as well as the positions of alignment marks b of the chips S_B and S_C (or alignment marks b' of the chips S_A and S_D) are measured. Based on this, it is possible to calculate the chip magnification in respect to each of the X and Y directions. On the other hand, by measuring the positions of alignment marks b' of the chip S_A and alignment mark b of the chip S_B. it is possible to calculate the chip rotation.

The chip magnification error can be corrected by adjusting a portion of the exposure optical system 103. Also, the chip rotation can be corrected by rotating the wafer during the step-and-repeat motion of the wafer stage 107, in accordance with the calculation result. Thus, even in large-field 'exposure process. further enhancement of the alignment precision is assured.

Figure 16 is a plan view of a reticle according to a further embodiment of the present invention. Figure 17 is a plan view for explaining exposure layout in a case where the exposure process is to be made by using the above reticle. In this example, alignment marks a, b. a' and b' are placed at corner portions of chip patterns. which are on diagonals of the exposure filed. The alignment mark span in the measurement of chip magnification or chip rotation is larger than that of the embodiment of Figure 14. Also in this embodiment. correction of chip rotation or chip magnification is attainable through measurement using alignment marks a. b. a' and b'. as has been described with reference to the Figure 14 embodiment.

While the invention has been described with reference to the structures disclosed herein. it is not confined to the details set forth and this application is intended to cover such modifications or changes as may come within the purposes of the improvements or the scope of the following claims.

Claims

1. An alignment method in an exposure process in which a first stepper having a first reduction magnification and a second stepper having a second reduction magnification. higher than the first reduction magnification. are used in combination. characterized in that:

   for a global alignment through the first stepper on the basis of alignment marks having been defined through the second stepper in relation to shots thereof, in every shot of the first stepper the position of such alignment mark or marks to be measured is made variable with respect to the shot center.

2. A method according to Claim 1, wherein in the global alignment through the first stepper. the same alignment mark to be used in global alignment through the second stepper is measured.

3. An alignment method in an exposure process in which a first stepper having a first reduction 'magnification and a second stepper having a second reduction magnification, higher than the first reduction magnification. are used in combination. characterized in that:

   for a global alignment through the second stepper on the basis of alignment marks having been defined through the first stepper, in every shot of the second stepper the position of such alignment mark or marks to be measured is made variable with respect to the shot center.

4. A method according to Claim 3, wherein alignment marks defined through the first stepper are placed symmetrically with respect to the shot center of the first stepper. and wherein the global alignment through the second stepper uses the thus symmetrically placed alignment marks the number of which is even for different shots.

5. A method according to Claim 3. wherein alignment marks of a shot of the first stepper are placed symmetrically in a direction of measurement and with respect to the shot center, and wherein the number of alignment marks to be measured in relation to the symmetrical pair is even.

6. An alignment method in an exposure process in 'which alignment marks are formed on a substrate and in which a first stepper having a first reduction magnification and a second stepper having a second reduction magnification, higher than the first reduction magnification. are used in combination. characterized in that:

offsets are set on the basis of image heights of alignment marks of a shot, and wherein the set offset are reflected in accordance with the number of alignment marks at each image height as measured.

7. A reticle to be used in a semiconductor exposure apparatus and having a pattern of plural chips to be exposed in relation to a single shot, characterized in that:

   the reticle is provided with an alignment mark in relation to each of the chips.

8. An exposure method for performing sequential exposure of different shot regions of a substrate, comprising the steps of:

   performing an exposure process to the substrate by use of a reticle having plural chip patterns, to be exposed in a single shot, and alignment marks provided in relation to the chip patterns, respectively: and
   performing an alignment process to the substrate by using an alignment mark in each chip as transferred to the substrate through said exposure process.

9. A method according to Claim 8, wherein, in each shot on the substrate, a position measurement error produced in dependence upon the position of an alignment mark with respect to the shot center is measured and wherein a measured value of each alignment mark position with respect to the shot center is corrected on the basis of the error measurement.

10. A method according to Claim 8. wherein the alignment process is a global alignment process.

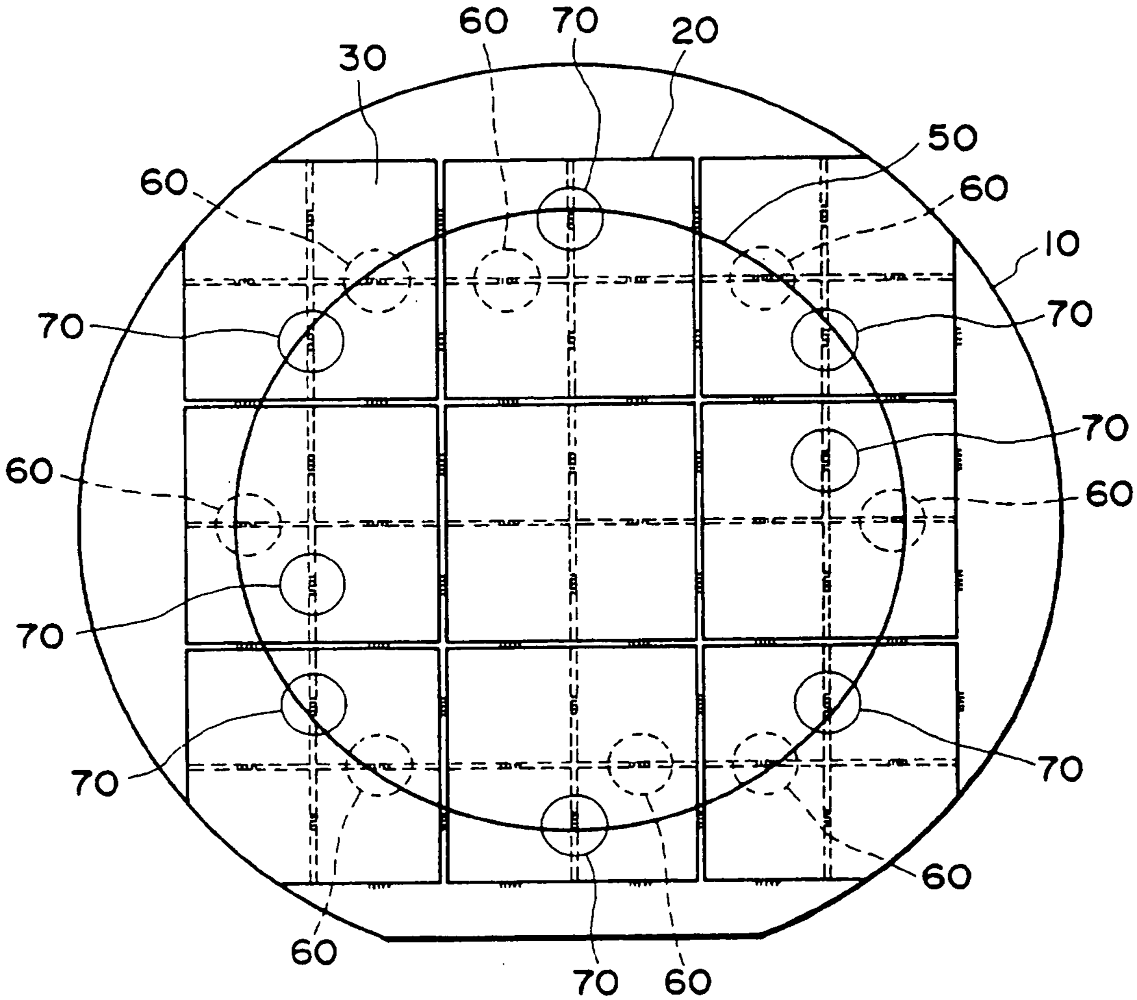
11. An exposure method for performing sequential exposure of different shot regions of a substrate, comprising the steps of:

    performing an exposure process to the substrate by use of a reticle having plural chip patterns, to be exposed in a single shot, and alignment marks provided in relation to the chip patterns, respectively: and
    measuring at least one of a chip magnification error and a chip rotation, by using an alignment mark in each chip as transferred to the 'substrate through said exposure process.

12. A method according to Claim 11, wherein each chip of the reticle is provided with two opposed alignment marks for X-direction detection and two opposed alignment marks for Y-direction detection, which are disposed around that chip.

13. A method of producing a semiconductor device wherein a reticle is aligned in relation to a wafer and a pattern on the reticle is transferred to the wafer by step and repeat exposure, wherein alignment of the reticle is performed by any method as claimed in claims 1 to 6.

14. A method of producing a semiconductor device wherein sequential exposure of different slot regions is performed by an exposure method as claimed in any of claims 8 to 12.



30
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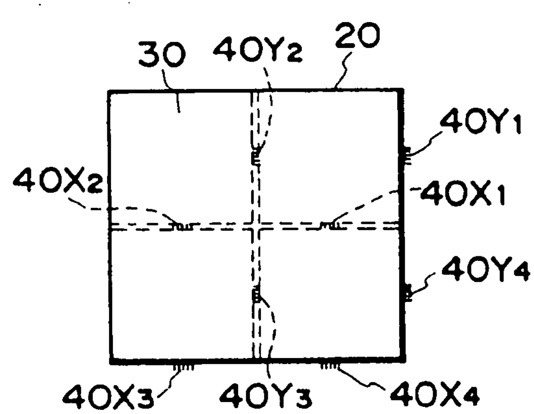
60

FIG. 1



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40Y2
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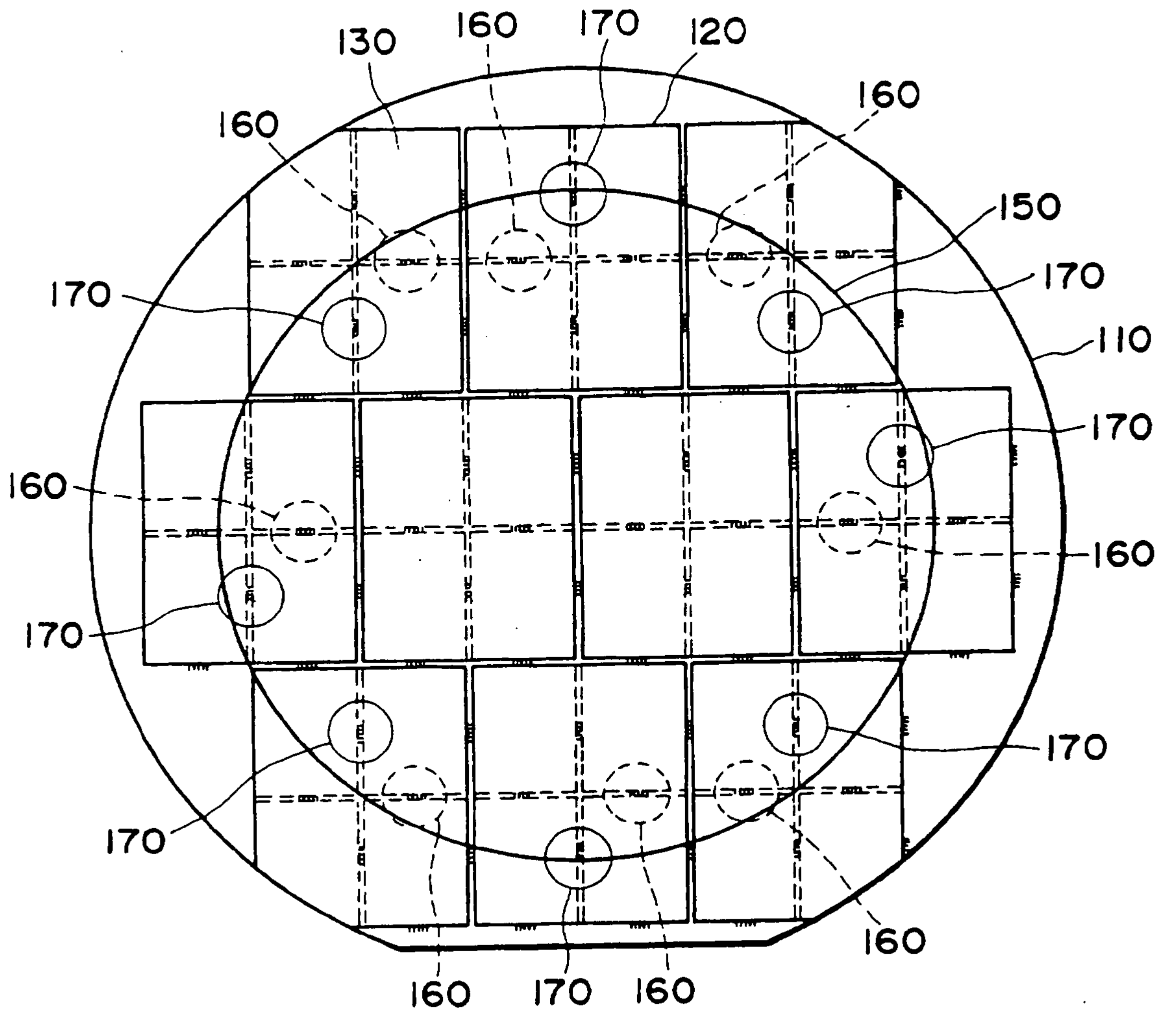
40Y1
40X2
40X1
40Y4
40X3
40Y3
40X4

FIG. 2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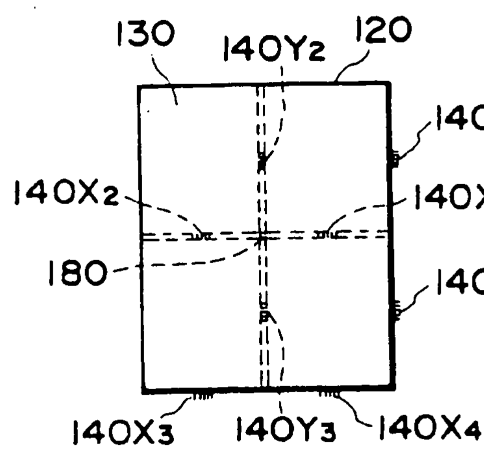
160

FIG. 3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140X1
180
140Y4
140X3
140Y3
140X4

FIG. 4

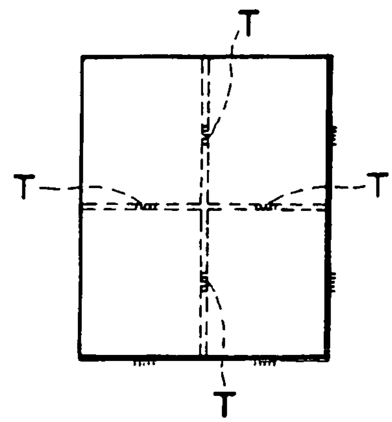


FIG. 5

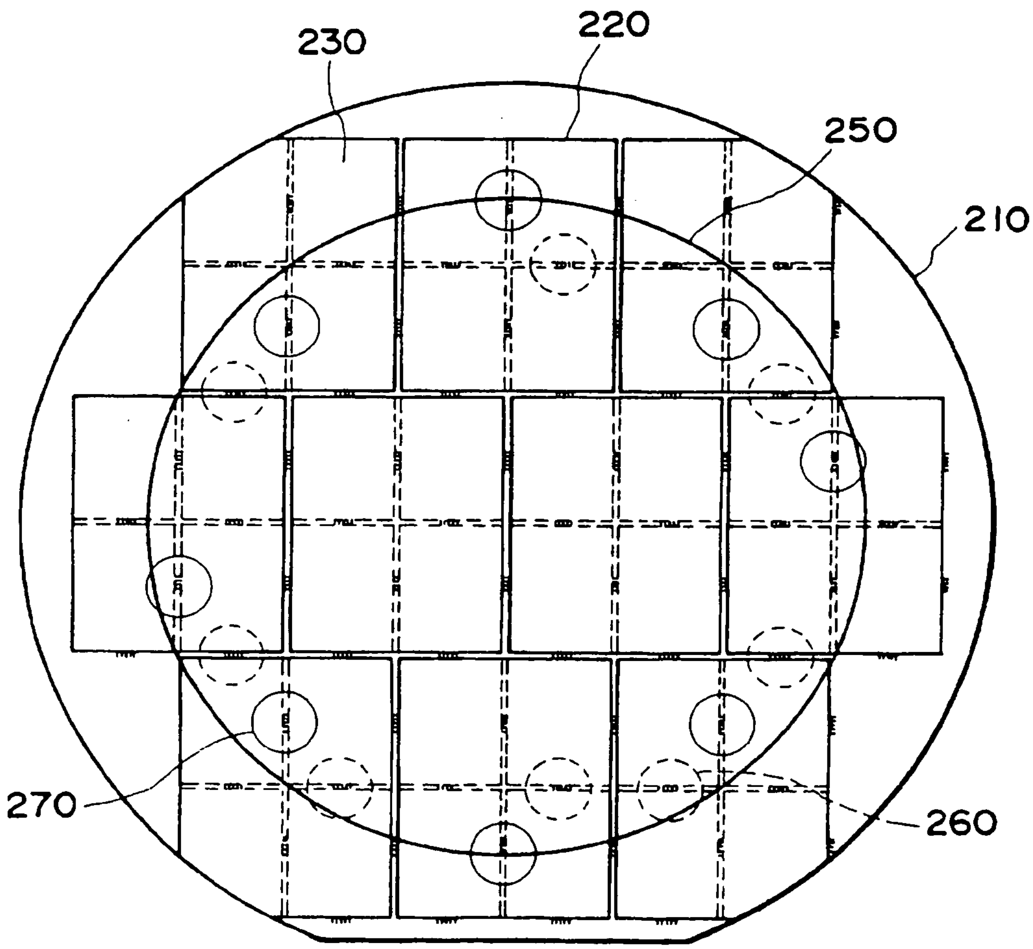
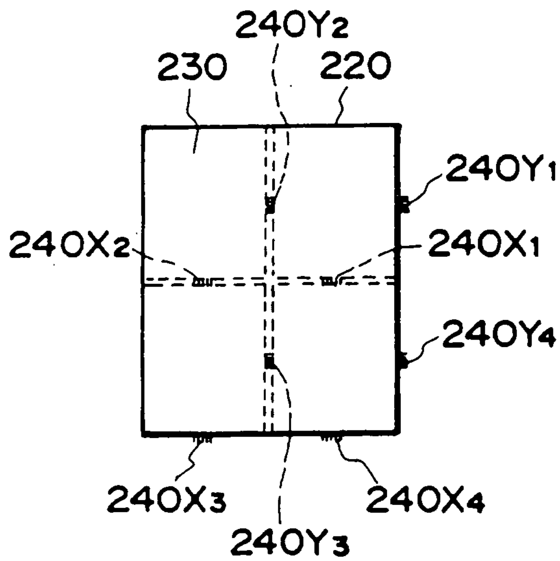


FIG. 6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240Y1
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240Y4
240X3
240X4
240Y3

FIG. 7

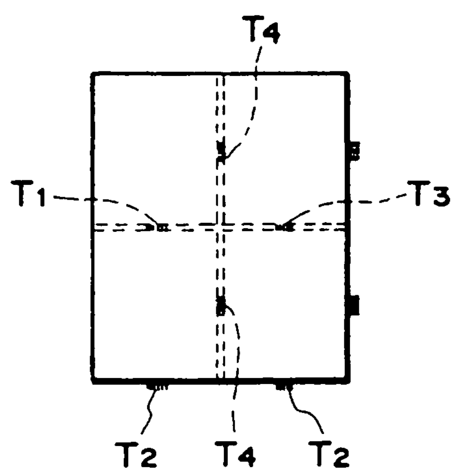

T4
T1
T3
T2
T4
T2

FIG. 8

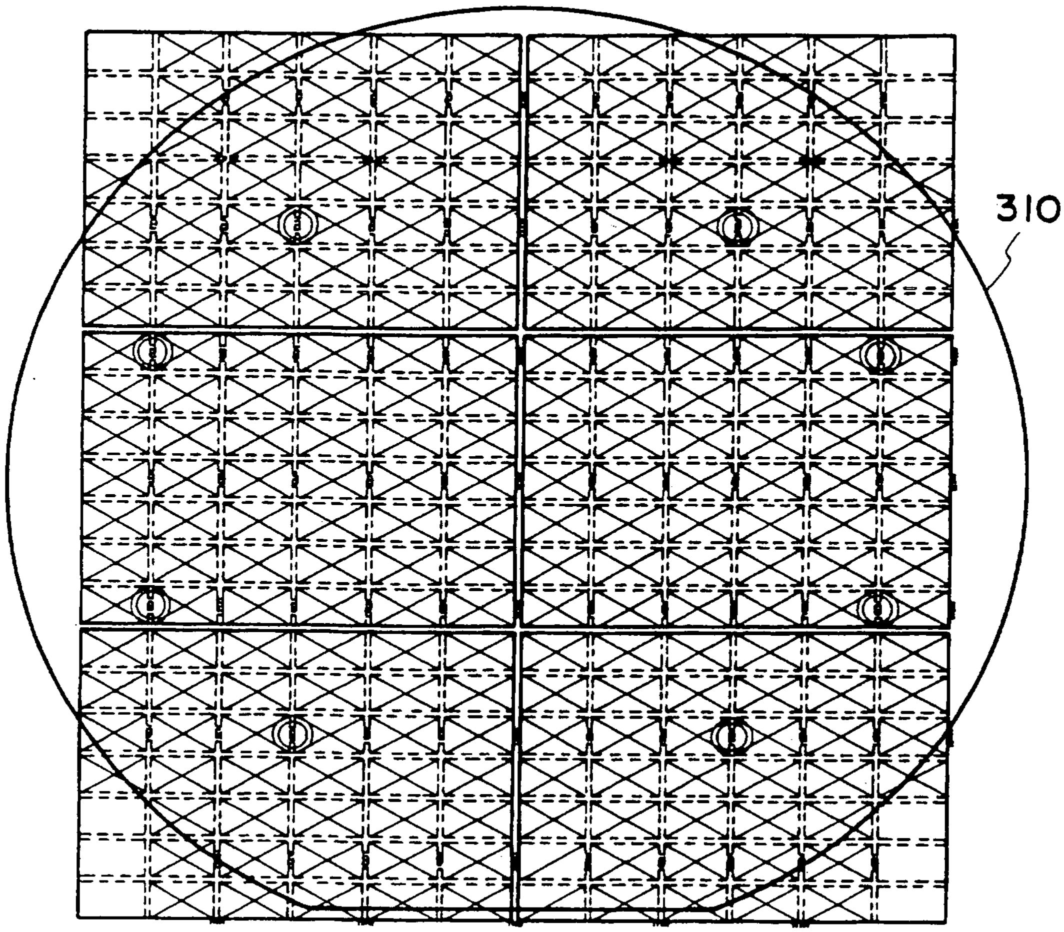


FIG. 9

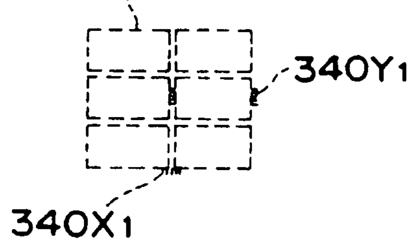


FIG. 10

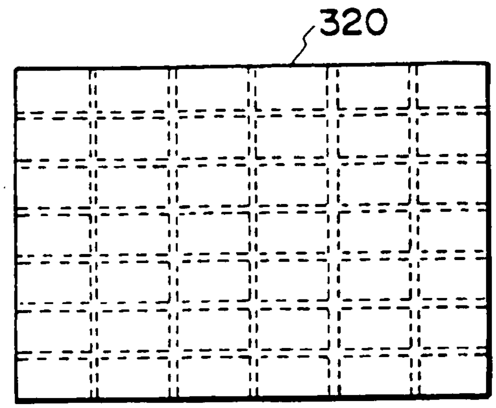


FIG. 11

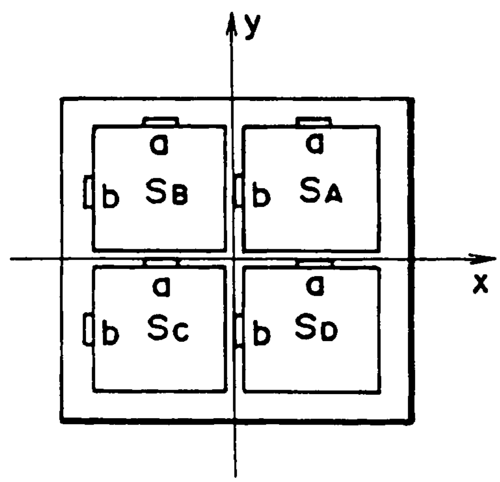


FIG. 12

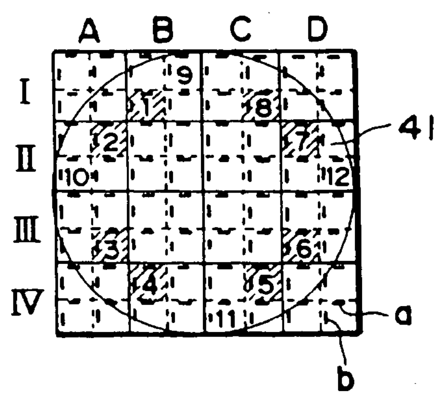
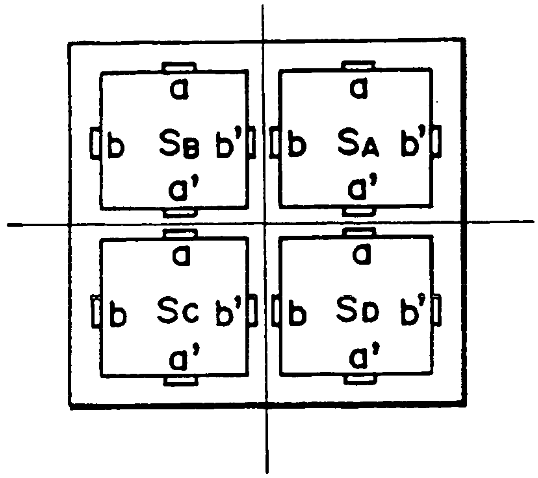


FIG. 13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b
SB
b'
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b
Sc
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a'
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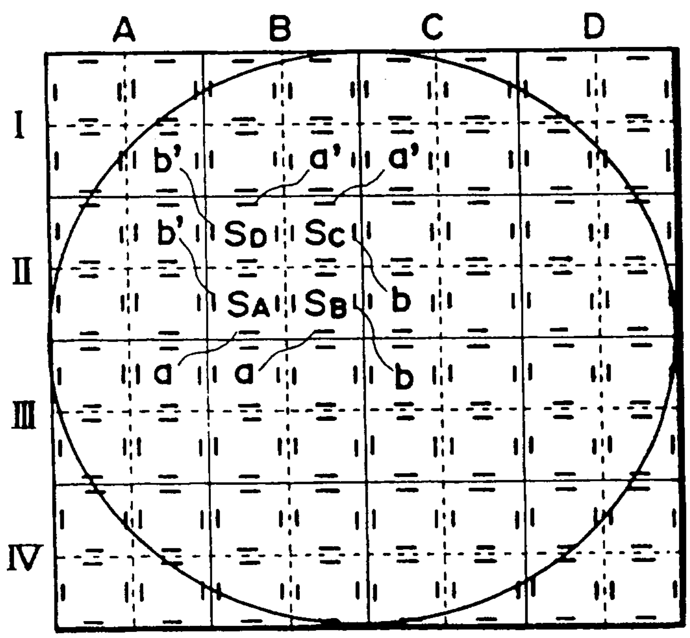
SD
b'
a'

FIG. 14


A
B
C
D
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III
IV
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SD
Sc
SA
SB
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a
b

FIG. 15

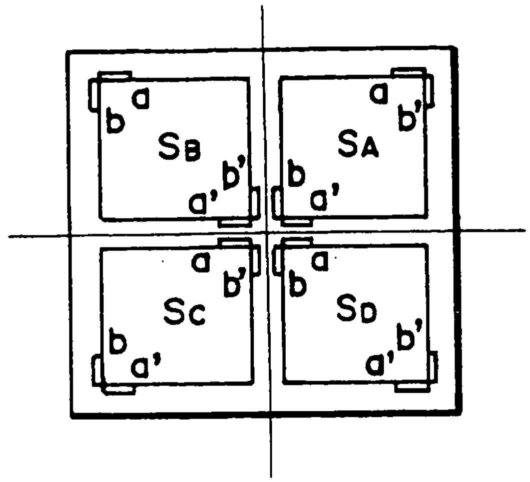

FIG. 16

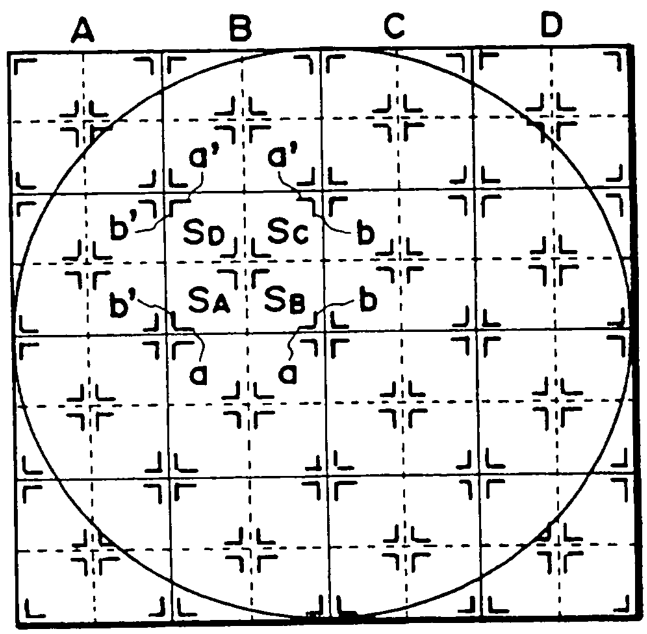

FIG. 17

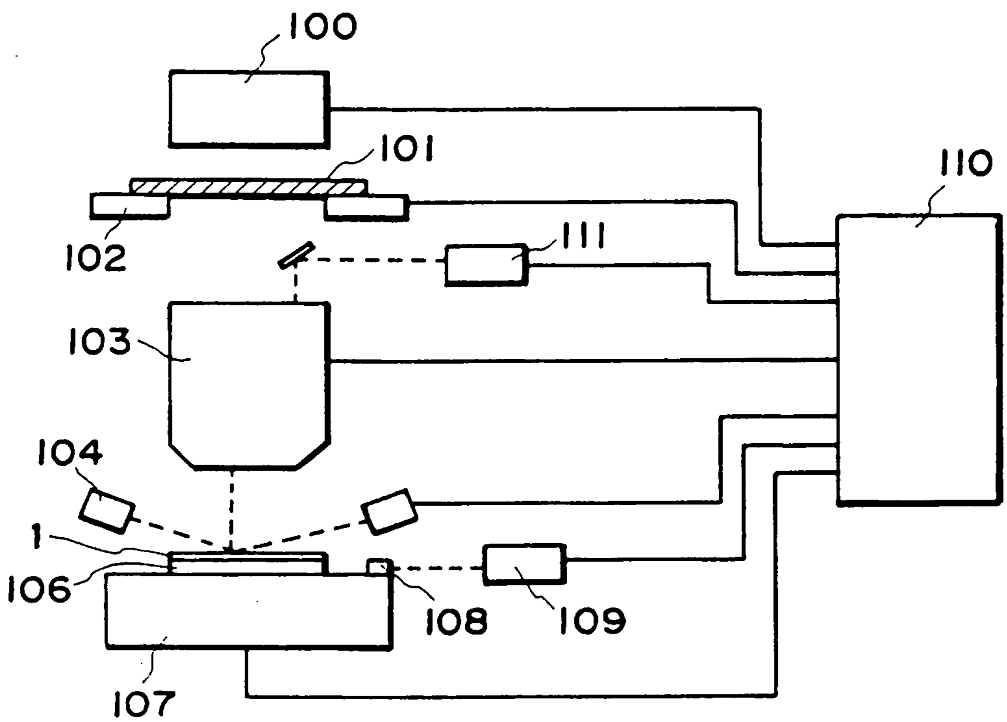

FIG. 18

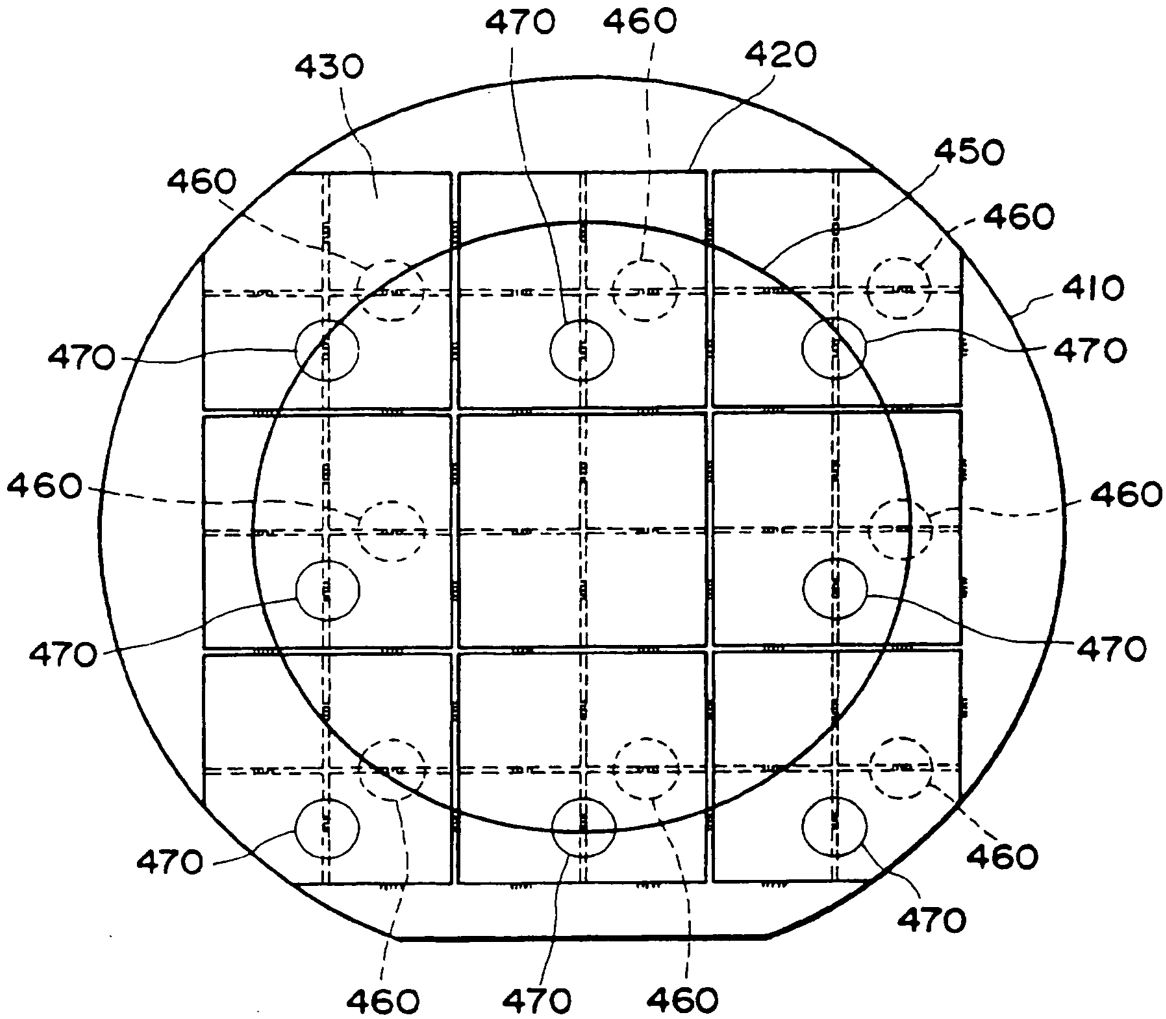
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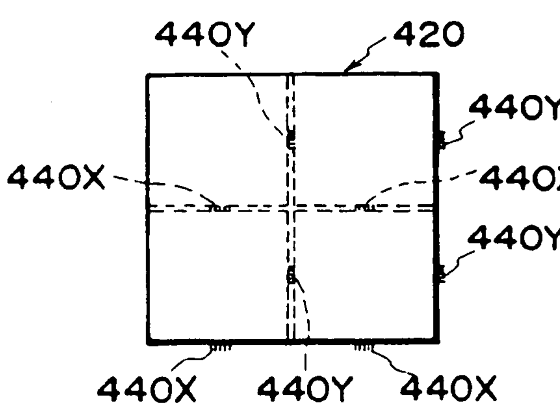
FIG. 19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440Y
440X
440Y
440X

FIG. 20

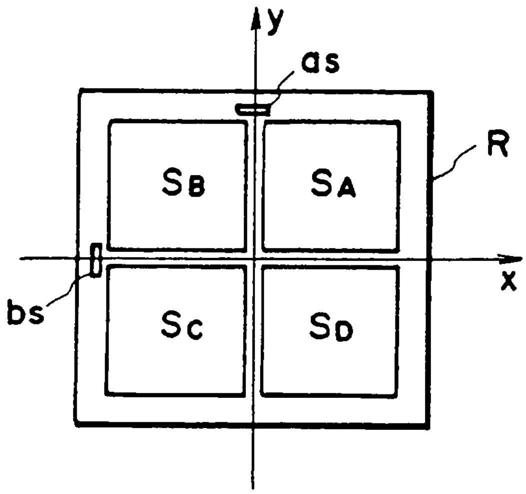

FIG. 21

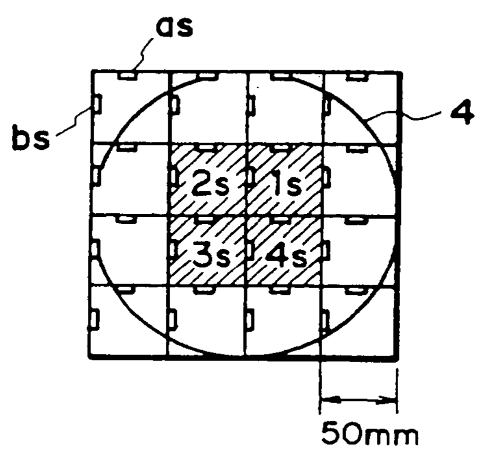

FIG. 22

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 30 8529

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US-A-5 250 983 (YAMAMURA RYUJI) 5 October 1993 * column 3, line 32 - column 4, line 22 * * figures 4-6 *	7,8,11, 12,14	G03F9/00 G03F7/20
X	EP-A-0 440 470 (CANON KK) 7 August 1991 * column 8, line 53 - column 10, line 48 * * figures 1-4,8 *	7,8,14	
A	US-A-4 734 746 (USHIDA KAZUO ET AL) 29 March 1988 * column 3, line 29 - column 7, line 56; figures 1-7 * * column 19, line 45 - column 20, line 32; figures 23,24 * * column 23, line 32 - column 25, line 41; figure 31 *	1,3,6, 11,13,14	
A	PATENT ABSTRACTS OF JAPAN vol. 018 no. 545 (E-1617) ,18 October 1994 & JP-A-06 196384 (NIKON CORP) 15 July 1994, & US-A-5 448 333 (IWAMOTO YOSHICHIKA ET AL) 5 September 1995 * column 5, line 51 - column 12, line 58 * * figures 1-3,8,9 *	1,3,6, 11,13,14	TECHNICAL FIELDS SEARCHED (Int.Cl.6) G03F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	7 March 1996	Heryet, C

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
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E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document